Reg.No.:

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70056

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JAN. / FEB. 2026
First Semester
VLSI Design
P23VD101 - ANALOG IC DESIGN
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

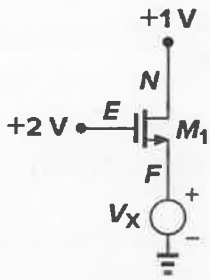
Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

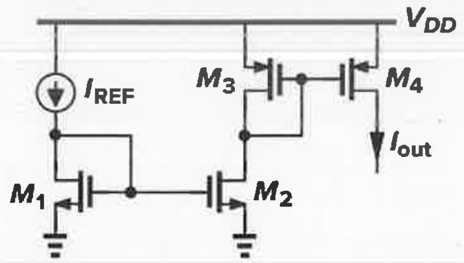
PART – A

(10 x 2 = 20 Marks)

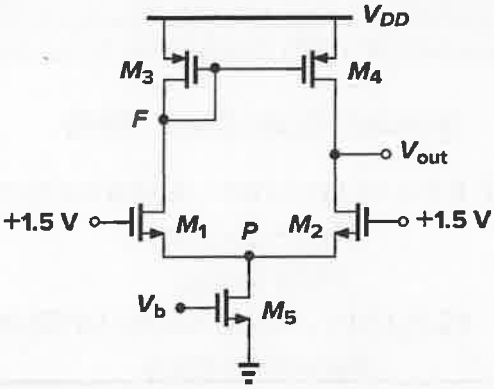
Q.No.	Questions	Marks	KL	CO
1.	Sketch the capacitances of M_1 (C_{EN} and C_{EF}) as V_X varies from zero to 3 V. Assume that V_{TH} = 0.3 V and $\lambda = \gamma = 0$.	2	K2	CO1



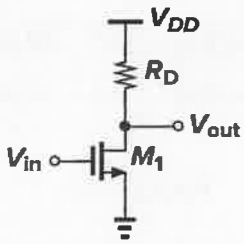
Q.No.	Questions	Marks	KL	CO
2.	Keeping all other parameters constant, plot the I_D/V_{DS} characteristic of a MOSFET for $L = L_1$ and $L = 2L_1$.	2	K2	CO1
3.	Find the drain current of M_4 if all of the transistors are in saturation.	2	K2	CO2



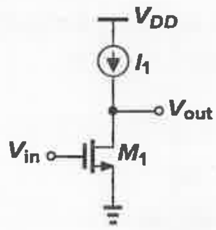
4. Assuming perfect symmetry, sketch the output voltage of the circuit as V_{DD} varies from 3 V to zero. Assume that for $V_{DD} = 3$ V, all of the devices are saturated. — 2 — K2 — CO2



5. Sketch the drain current and transconductance of M_1 as a function of the input voltage. — 2 — K2 — CO3



6. Assuming that M_1 is biased in saturation, calculate the small-signal voltage gain of the circuit. — 2 — K2 — CO3



7. Define spurious-free dynamic range (SFDR) in DAC/ADC evaluation. — 2 — K1 — CO4

8. Define settling time of a DAC. — 2 — K1 — CO4

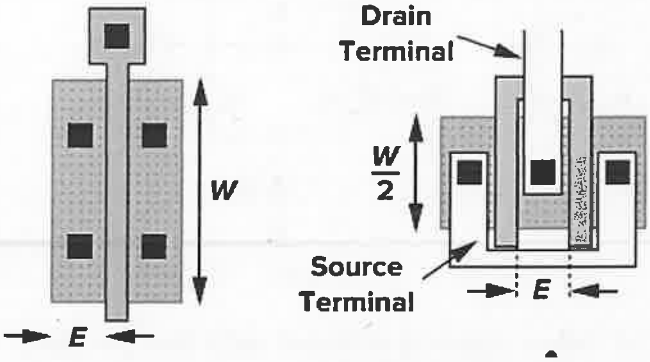
9. Define regeneration in latch comparators. — 2 — K1 — CO5

10. Explain the impact of kickback noise in high-speed comparators. — 2 — K2 — CO5

PART – B

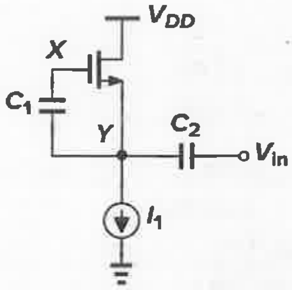
(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Calculate the source and drain junction capacitances of the two structures. Compare the drain junction capacitance of each structure.	13	K3	CO1

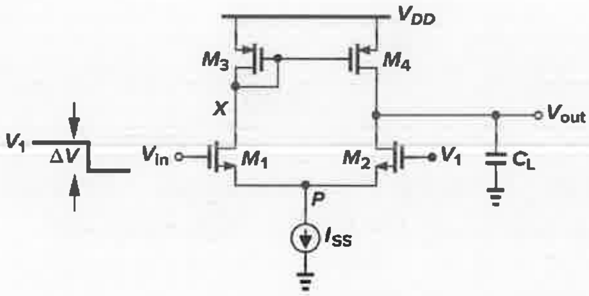


(OR)

	b)	Consider the circuit shown below, where the initial voltage at node X is equal to V_{DD}. Assuming that $\lambda = \gamma = 0$ and neglecting other capacitances, plot V_X and V_Y versus time if (a) Vin is a positive step with amplitude $V_0 > V_{TH}$, and (b) Vin is a negative step with amplitude $V_0 = V_{TH}$.	13	K2	CO1

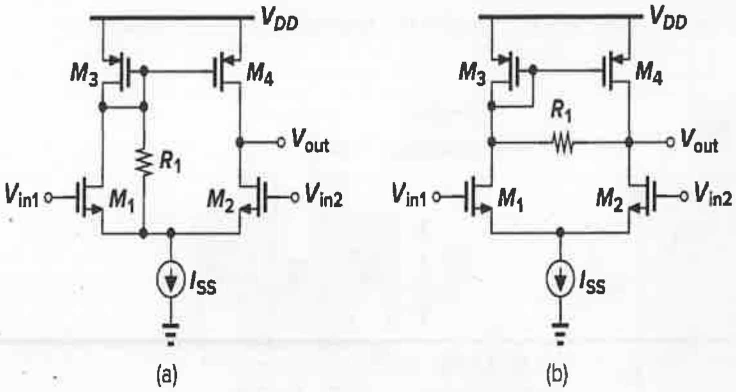


12.	a)	If in the below figure, ΔV is small enough that all of the transistors remain in saturation, determine the time constant and the initial and final values of V_{out}.	13	K4	CO2



(OR)

b) Due to a manufacturing defect, a large parasitic resistance, R_1, has appeared in the below circuits. Calculate the gain of each circuit if $\lambda > 0$. 13 K4 CO2

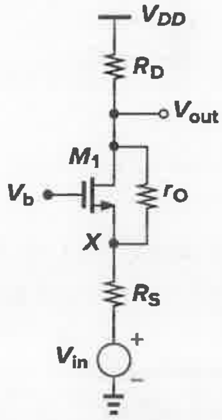


13. a) The CG stage of below figure is designed such that its input resistance (seen at node X) matches the signal source resistance, R_S. If $\lambda, \gamma > 0$, prove that 13 K3 CO3

$$\frac{V_{out}}{V_{in}} = \frac{1 + (g_m + g_{mb})r_O}{2 + \left(1 + \frac{r_O}{R_D}\right)}$$

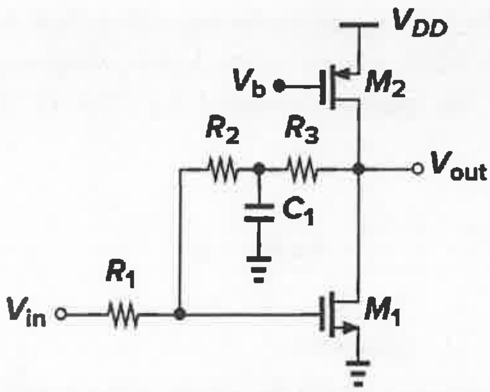
Also, prove that

$$\frac{V_{out}}{V_{in}} = \frac{R_D}{2R_S}$$



(OR)

b) In the below circuit, assume that $\lambda = 0$, $g_{m1,2} = 1/(200\ \Omega)$, $R_{1-3} = 2$ kΩ, and $C_1 = 100$ pF. Neglecting other capacitances, estimate the closed-loop voltage gain at very low and very high frequencies. 13 K3 CO3



14. a)	Explain the working principle of N-bit SAR ADC. Perform the operation of a 3-bit successive approximation ADC with V_{REF} = 8v. Make a table that consists of D_2,D_1,D_0,B_2,B_1,B_0,V_{OUT} (the output from the DAC) and the comparator output, which shows the binary search algorithm of the converter for V_{IN}=5.5 V and 2.5 V.	13	K3	CO4
	(OR)			
b)	A 4-bit Flash ADC converter has a resistor string with mismatch as shown in Table below. Determine the DNL and INL of the converter. How many bits of resolution does this converter possess? V_{REF}= 5 V.	13	K3	CO4

Resistor	Mismatch (%)
1	2
2	1.5
3	0
4	−1
5	−0.5
6	1
7	1.5
8	2
9	2.5
10	1
11	−0.5
12	−1.5
13	−2
14	0
15	1
16	1

15. a)	Design an open-loop comparator having pre-amplifier stage, latch stage and buffer output stage. Calculate the switching point for the low and high transition.	13	K2	CO5
	(OR)			

b)	Design a low power clocked comparator for use with a Flash ADC. Use the short-channel CMOS process and a clocking frequency of 250 MHz. Estimate the power dissipated by 256 of these comparators.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.	Questions	Marks	KL	CO
16. a)	Design a 3-bit Flash converter, listing the values of the voltages at each resistor tap, and draw the transfer curve for V_{IN}= 0 to 5V. Assume V_{REF} = 5V. Construct a table listing the values of the thermometer code and the output of the decoder for V_{IN} =1.5, 3.0, and 4.5V. Also, determine the maximum offset voltage of the comparators which will make the INL less than 1/2 LSB. Assume that the resistor string is perfectly matched.	15	K3	CO4
	(OR)			
b)	Design an 8-bit current-steering DAC using binary-weighted current sources. Assume that the smallest current source will have a value of 1 μA. Determine the range of values that the current source corresponding to the MSB can have while maintaining an INL of ½ LSB. Repeat for a DNL less than or equal to 1/2 LSB.	15	K3	CO4